Abstract of the Disclosure

A DLL circuit includes a delay circuit, a phase comparing circuit and a delay control circuit. The delay circuit is connected to first and second nodes, and delays an original clock signal supplied to the first node based on a delay control signal and generates first to n-th (n is an integer more than 1) internal clock signals. The first internal clock signal is outputted from the second node. Also, the internal clock signals other than the first internal clock signal are outputted from the delay circuit without passing through the second node, and lead the first internal clock signal in phase. The phase comparing circuit compares the original clock signal supplied from the first node and the first internal clock signal supplied from the second node, and outputs a phase difference of the original clock signal and the first internal clock signal. The delay control circuit outputs the delay control signal to the delay circuit based on the phase difference outputted from the phase comparing circuit.